Automated generation of high-quality PDKs to support academic research related to chip design

Summary

Computer chips are designed according to specific foundry recipes that specify what the allowable dimensions for transistors and metals are. The recipes are encoded as a Process Design Kit (PDK) that chip designers gain access only through NDAs. In response to this limitation, researchers have created academic PDKs that mimic industry PDKs to a limited capacity. These academic PDKs are, unfortunately, one-off solutions and the effort must be repeated every time a new academic PDK is created. The topic of this PhD thesis is precisely on how to automate the generation of high-quality PDKs to support academic research related to chip design.

Research field:	Information and communication technology
Supervisors:	Jaan Raik Samuel Pagliarini
Availability:	This position is available.
Offered by:	School of Information Technologies Department of Computer Systems
Application deadline:	Applications are accepted between October 01, 2024 00:00 and October 25, 2024 23:59 (Europe/Zurich)

Description

A high-quality PDK contains several assets that allow for chip design to be carried out in state-of-the-art physical synthesis tools. Those assets include:

- Technology description in LEF format
- Cell library description in LEF format
- Cell library characterization in LIB format
- Collaterals for timing analysis and physical verification, including extraction rules and DRC decks
- SPICE models for transistors

With the exception of cell library characterization that is already automated, all other files are generated with a high degree of human interaction because a PDK generator does not exist today. We hypothesize that possessing a PDK generator capable of understanding all these file formats would enable researchers to much more effectively create new technologies for use in academia and industry. Furthermore, this line of research is very timely with all the open-source initiatives in the European chip design ecosystem.

Once the generator is in place, the avenues for future research increase manyfold. The ability to quickly modify and generate an updated PDK will enable true Design-Technology Co-Optimization (DTCO). Decisions such as pinout of cells, cell height, power rails, and many more, can be quickly evaluated with near zero effort. Today, once a design house decides to fabricate a chip, it takes the cell library as a constraint that must be respected. Yet, this cell library is optimized for an average design and may not represent the best optimization point. With the aid of a PDK generator, thousands of versions of the same design can be evaluated with tweaks to the PDK/library that benefit that specific design, finally enabling a high-fidelity high-precision design space exploration framework for chip design.

Furthermore, the PDK generator can also be used to explore emerging technologies and how they interplay with traditional CMOS. It can be used to evaluate 3D stacking of dies, chiplets, MRAM, RRAM, photonics, and many others.

Applicants should fulfil the following requirements:

- a master’s degree in computer science, computer engineering, electrical engineering or similar areas
- a clear interest in the topic of the position
- excellent command of written and oral English
- strong and demonstrable writing and analytical skills
- capacity to work both as an independent researcher and as part of an international team

The following experience is considered beneficial:

The ideal candidate should have a master's degree in electrical or computer engineering with an emphasis on VLSI/CAD. The candidate should also have programming skills in C/C++ and/or Python for automation. Familiarity with Cadence/Synopsys design flows is also highly sought.

We offer:

- A 4-year PhD position in one of the leading nanoelectronics research centers in Europe with a large portfolio of ongoing pan-European and national research and innovation projects
- Competitive salary and generous leave
- The chance to do high-level research in one of the most dynamic digital government contexts globally
- Opportunities for conference visits, research stays and networking with globally leading universities and research centers
- Opportunity to fabricate chips in order to validate the research, in cooperation with commercial foundries

About the Department

The Department of Computer Systems focuses on the areas of design of dependable computing systems, including reliability, verification and testing of nanoelectronic systems, intelligent and control systems, virtual reality, and biorobotics. The department is highly engaged in international cooperation in research, and provides teaching through all study levels – bachelor's, master's and doctoral studies.

About Taltech

TalTech - Tallinn University of Technology (https://www.taltech.ee/en/) is an internationally recognized research university located in the beautiful Tallinn, Estonia. As the flagship of Estonian engineering and technical education, TalTech offers high-quality education in various fields such as technological, natural, exact, social, and health sciences. With a mission to develop the economy and industry of the Baltic Sea region, TalTech provides an inspiring environment for students with exciting cultural and sporting activities.

About Estonia:

Estonia is a true digital society. In just 20 years, Estonia has become one of the most technologically advanced societies in the world. Some of the fastest broadband speeds in the world are widely available across the country. But more importantly, so is the wireless Internet which covers everything.

In Estonia you are never more than a 30-minute drive away from a forest or a lake. The living environment is very clean, relaxed and safe. According to the World Health Organization, Estonia has the best overall air quality in the entire world.

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