Reliable RISC-V-based architectures for Edge AI

Summary

The PhD project aims at novel, low-cost, ultra-low power open-source RISC-V-based accelerators augmented with reliability and safety features and tailored for edge AI applications. Energy efficiency is to be addressed by optimisation of the architecture, memory communication and the control. The lifetime and soft-error reliability aspect assumes architectural and physical design methodologies, as well as system-level improvements. For safety, the development of an infrastructure for in-field fault management of RISC-V-based systems to prevent catastrophic system failures, including fault and ageing detection and recovery mechanisms, using IJTAG for embedded instruments. This PhD position is one of the 17 positions in the European Marie Skłodowska-Curie Action Doctoral network "TIRAMISU - Training and Innovation in Reliable and Efficient Chip Design for Edge AI" (2024-2028).

Research field:	Information and communication technology
Supervisors:	Prof. Dr. Maksim Jenihhin Dr. Artur Jutman Dr. Jürgen Alt
Availability:	This position is available.
Offered by:	Tallinn University of Technology School of Information Technologies
Application deadline:	Applications are accepted between September 01, 2024 00:00 and October 31, 2024 23:59 (Europe/Zurich)

Description

The research

Very recently, the landscape of Artificial Intelligence (AI) development has undergone a remarkable transformation, marked by the trend of fusion of AI with the edge computing concept. Artificial intelligence is increasingly being brought to the source of data, i.e., the devices at the network's edge, thus establishing the Edge AI concept. Edge AI is gaining momentum across various industries and services by public authorities because it enables new applications requiring high performance, ultra-low latency with high bandwidth, efficient power use, and intelligence beyond regular computing.

The PhD project aims at novel, low-cost, ultra-low power open-source RISC-V-based accelerators augmented with reliability and safety features and tailored for Edge AI applications. Energy efficiency is to be addressed by optimization of the architecture, memory communication and the control. The lifetime and soft-error reliability aspect assumes architectural and physical design methodologies, as well as system-level improvements. For safety, the development of an infrastructure for in-field fault management of RISC-V-based systems to prevent catastrophic system failures, including fault and ageing detection and recovery mechanisms, using IJTAG for embedded instruments.

This position is a part of new European MSCA Doctoral Network TIRAMISU "Training and Innovation in Reliable and Efficient Chip Design for Edge AI" (2024-2028) https://tiramisu-project.eu/. The action will provide strong interdisciplinary training for future European engineers and researchers driving the innovation for reliable and energy-efficient Edge AI chips. The consortium is strategically designed to foster cross-disciplinary synergies, by seamlessly integrating innovation management research with the technical aspects of Edge AI design. The non-academic sector is represented by a European flagship R&D hub for nanoelectronics - IMEC, a global leader in industrial electronics and the largest semiconductor manufacturer in Germany - Infineon, a trusted automotive solutions provider - Dumarey, the worldwide leader in EDA tools development - Cadence. The academic excellence is established by the top ICT and Technology Innovation engineering universities and Europe's largest application-oriented research organisation - Fraunhofer.

Applicants should fulfil the following requirements:

- (MSCA DN Mobility Rule) **Applicants must not have resided or carried out their main activity (work, studies, etc.) in Estonia for more than 12 months in the 36 months immediately before their date of recruitment.**

Compulsory national service, short stays such as holidays, and time spent as part of a procedure for obtaining refugee status under the Geneva Convention are not taken into account. Date of Recruitment means the first day of the employment of the researcher for the purposes of the action (i.e. the starting date indicated in the employment contract or equivalent direct contract).

- a master's degree (or equivalent) degree in Computer Engineering, Computer Science, Artificial intelligence or related areas.
- a clear interest in the topic of the position (candidates with embedded systems and machine learning backgrounds are preferred)
- basic understanding of reliability and machine learning concepts
- good skills in VHDL or Verilog
- ability to code in C/C++ or Python
- English language proficiency
- strong writing and communication skills compatible with an entry-level research position
- capacity to work both as an independent researcher and as part of an international team
- capacity and willingness to provide assistance in organisational tasks relevant to the project

The following experience is beneficial:

- research and/or professional experience, ability and interest to collaborate across disciplines
- familiarity with RISC-V architecture
- familiarity with FPGA development
- familiarity with EDA tools
- familiarity with ML algorithms and DNN architectures
- previous research publications at conferences or journals

The candidate should submit a research plan for the topic. The candidate can expand on the outlined research scope and propose theoretical lenses to be used.

We offer:

- 4-year PhD position in the Department of Computer Systems that has a sound portfolio of ongoing European and national research projects
- An environment to do excellent research and publications
- Opportunities for training relevant technical and transferable skills aiming academic or industrial careers
- Opportunities for conference visits, research stays and networking with globally leading companies, universities and research centres in the field of research

About the department

The Centre for Trustworthy and Efficient Computing Hardware (TECH) belongs to the Department of Computer Systems. It focuses on cross-layer reliability and self-health awareness technology for tomorrow's complex intelligent autonomous systems and IoT edge devices in Estonia and the EU. The team studies advanced cyber-physical systems characterised by their heterogeneity and emerging computing architectures employing AI-based autonomy. The centre generates knowledge to equip engineers with design-phase solutions and in-field instruments for industry-scale systems to facilitate the system's crashless operation. The core competencies of TECH are: Hardware design; VHDL and Verilog designs; EDA tools (Cadence, Siemens, Synopsys platforms); Application-specific computing platforms (Unmanned Aerial Vehicles); FPGA-based solutions and methodologies; Advanced FPGA SoCs and FPGA development tools (Xilinx Vivado, Altera/Intel Quartus, Lattice Diamond); Software and embedded SW development; Bare-metal and User-space applications; Cross-layer reliability and fault management; ML-based solutions; Functional Safety (ISO26262); Test strategy development and troubleshooting instrumentation; JTAG/IJTAG based solutions; RISC-V processor architectures; DNN hardware accelerators. Head of the centre: Prof. Maksim Jenihhin.
Prof. Maksim Jenihhin is a tenured associate professor of Computing Systems Reliability at the Department of Computer Systems of Tallinn University of Technology and the head of the research group "Trustworthy and Efficient Computing Hardware". He received his Ph.D. degree in Computer Engineering from the same university in 2008. His research interests include methodologies and EDA tools for hardware design, verification and debugging as well as nanoelectronics reliability and manufacturing test topics. He supervised 5 PhD theses on these topics and published more than 170 peer-reviewed publications. He is a coordinator for national and European research projects,

including Horizon MSCA DN TIRAMISU (2024-2028), Horizon Twinning TAICHIP (2024-2027), H2020 MSCA ITN RESCUE (2017-2021), PRG 2022 CRASHLESS (2022-2027). Prof. Jenihhin is a member of executive and program committees for IEEE ETS, DATE, DDECS, and a number of other international events and served as a guest editor for special issues of journals.

Dr. Artur Jutman has been managing industrial and research projects in Testonica Lab Ltd. for over 15 years now. His professional focus embraces such topics as diagnostic and defect modeling, test optimization, embedded test instrumentation, test firmware, BIST, DFT as well as both ASIC and system test in a broad sense - all yielding over 160 peer-reviewed research papers published. Dr. Jutman has co-ordinated several EU-funded research projects on test-related topics, participated in organizing test conferences and workshops across Europe as well as given several keynotes, invited talks, embedded and full tutorials at international conferences and symposia. Dr. Artur Jutman received his M.Sc. and Ph.D. degrees in computer engineering from Tallinn University of Technology, Estonia in 1999 and 2004 respectively.

Dr. Juergen Alt is a Senior Principal Engineer at Infineon. Within Infineon's architecture group for Automotive Microcontrollers, he is responsible for test concept and Design-for-Test architecture of the next-generation microcontroller platform. He contributed to various university and industry collaboration projects. For Rescue European Training Network he served as a member of the industrial advisory board. During his more than 25 years in industry he supervised multiple master theses and other student's work. At Friedrich-Alexander University Erlangen, Germany he is lecturer for DfT courses, and he contributed to multiple conferences by regular presentations. Juergen Alt is based in Munich, Germany and has diploma and doctoral degrees in electrical engineering both from University of Hannover, Germany. For further information, please contact Prof Maksim Jenihhin (maksim.jenihhin@taltech.ee).

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