Cross-Layer Self-Health Management for Intelligent Autonomous Systems

Summary

The PhD project aims at new cross-layer reliability and self-health awareness technology for tomorrow's intelligent autonomous systems and IoT edge devices.

Research field:	Information and communication technology
Supervisors:	Prof. Dr. Maksim Jenihhin Dr. Artur Jutman
Availability:	This position is available.
Offered by:	School of Information Technologies Department of Computer Systems
Application deadline:	Applications are accepted between September 01, 2021 00:00 and September 30, 2021 23:59 (Europe/Zurich)

Description

Today, with the rise of AI, the electronic systems gradually become intelligent enough to become self-aware and situation-aware. These two concepts are being extensively studied today with active research and development work ongoing both in academia and industry. An important aspect in Self-Awareness is the ability of the system to comprehend and maintain its fitness in context of its goals and decisions as well as to adapt the decisions in accordance to the system fitness and the current situation. This specific ability is understood as Self-Health Awareness, which is also the next emerging paradigm on the path starting from the classic passive Fault Tolerance through Error Resilience and Fault Detection Isolation and Recovery (FDIR) towards intelligent reliability/safety management solutions. At the same time Self-Health Awareness is the cornerstone of several emerging offspring research directions, such as:

- Self-Healing
- Self-Adaptation to Damage
- Instant Failure Avoidance
- System Health Management
- AI-Driven Adaptive Predictive Maintenance

These research directions will have to be stdudied by the PhD candidate with subsequent achievement of publishable progress beyound the state-of-the-art through research activities in collaboration with other PhD students and staff at the Department of Computer Systems.

It is commonly understood by the research community that a self-adaptation framework has to hierarchically and systematically span across all system levels being distributed throughout the systems of systems (SoS), such as Internet-of-Things (IoT) or satellite constellations down to the level of individual agents like CPSs, computers, embedded systems, down to electronic blocks, incl. sensors and actuators, down to individual microcontrollers, CPUs/GPUs, memories, FPGAs and even further down to their sub-modules and sub-units. The particular aim of this study is to develop and evaluate the bottom up approach starting from the micro level upwards.

We are looking for motivated individuals with a strong background in hardware design.

The applicants are expected to demonstrate:

- Relevant technical education and training (candidates with embedded systems backgrounds are preferred)
- Basic understanding of reliability and artificial intelligence concepts
- Good skills in VHDL or Verilog
- Ability to code in C/C++ or Python
- Familiarity in FPGA development tools
- Writing and communicating skills (English) that are compatible with an entry-level research position
- English language proficiency
- Research and/or professional experience ability and interest to collaborate across disciplines

TalTech is an equal opportunity university. Female candidates are particularly encouraged to apply.

To get more information or to apply online, visit https://taltech.glowbase.com/positions/428 or scan the the code on the left with your smartphone.